## IN THE CLAIMS

1. (Currently Amended) A memory array, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

a number of bit lines coupled to the second source/drain region of at least one memory cell;

a number of wordlines coupled to the gate region of at least one memory cell;

a strapping line of lower resistance than the wordlines coupled to a single continuous wordline in a single array wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch; and

at least two channels connecting the strapping line to a first and second end of the portion of the single continuous wordline.

2. (Original) The memory array of claim 1 wherein the strapping line comprises metal.

3. (Original) The memory array of claim 2 wherein the metal comprises a refractory metal.

4. (Original) The memory array of claim 1 wherein the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline.

5. (Currently Amended) A memory array, comprising:

a number of memory cells having a first source/drain region and a second source/drain region and a gate region;

a number of source lines coupled to the first source/drain region of at least one memory cell;

Entry is denied - gl 08/10/04